A SiGe Transceiver Chipset for 100Mbps/1Gbps Digital Communication Over Cable System

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ABSTRACT — **In this paper we present the design and performance of transmit and receive SiGe RFICs that offer a complete RF transceiver solution to broadband digital communications over CATV cable system. The transceiver design is based on 16 QAM with direct modulation/demodulation approach, and which supports data speeds of 100 Mbps and 1 Gbps, using the frequency bandwidth of 900 MHz to 2.45 GHz. The Tx chip integrates DAC, Clock, LO, IQ modulator and RF transmitter, which offers linear output power of 7dBm and 1dBm at 1GHz and 2GHz, respectively. An output noise floor of -115dBm/Hz is also achieved. The Rx chips consist gain-switching LNA, RF VGA, RF slope equalizer, IQ demodulator, as well as clock, RF LOs, carrier recovery, AGC, clock recovery and ADC. With maximum gain setting, the entire Rx chain has a 20dB noise figure, which is critical in providing necessary dynamic range for such broadband communication. The VCO circuit on Tx/Rx chips is capable of switching between 4 separated frequencies with phase noise of –110dBc/Hz at 100kHz offset-carrier frequency. The chip-set has been successfully integrated into Narad Broadband Access Network (NBAN) system, which is currently under system test.**

I. INTRODUCTION

Increased demand for services such as high speed Internet access, VoIP, digital video, remote data storage, etc. fuels the need for true broad bandwidth with symmetric traffic, especially for the "last-mile" connection. Thus, Narad Broadband Access Network system [1]-[2] was developed to overcome the limits in conventional network access approaches, such as cable-modem (DOCSIS) and DSL [3]. These limits include bandwidth, symmetric traffic, security, dynamic network management and so on. NBAN (Narad Broadband Access Network) utilizes the bandwidth above 900 MHz in cable network for high-speed digital data communications. Existing CATV (legacy) system is compatible in NABN since at each port of cable nodes, high-speed data modulated RF signals are multiplexed/de-multiplexed with legacy signals. As shown in Fig.1, 100Mbps and 1Gbps signals are carried in 4 RF channels via 16QAM approach, spreading over 900MHz to 2.4GHz; bandwidth is approximately 60MHz and 600MHz for each 100Mbps and 1Gbps channel respectively. In NBAN system, modem circuits, capable of transmitting and receiving data signal at both 100Mbps and 1Gpbs, are required to enable data switching at each cable node. Thus, Tx/Rx RFICs were designed and fabricated using Atmel SiGe HBT process to provide high-speed performance with high dynamic range, low cost and low power-consumption for the modem circuit.

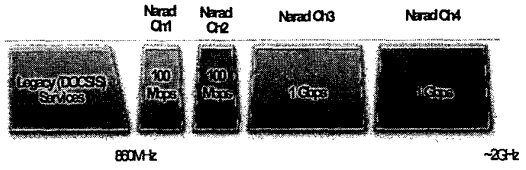
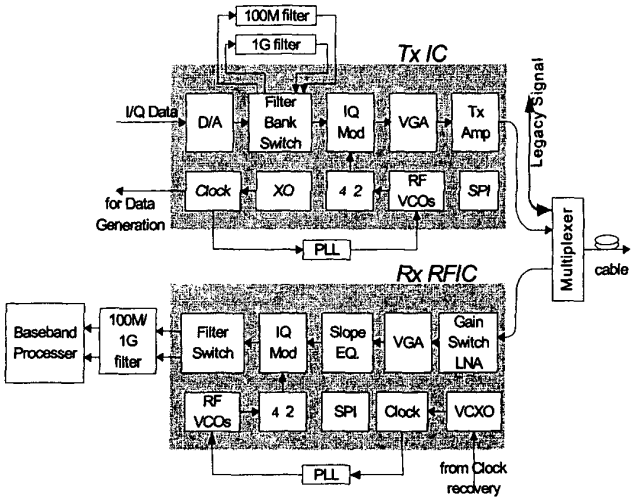


Fig.1 Frequency allocation in NBAN system.

This paper describes the basic functions, design, and measurement performance highlights of the transceiver chipset. Design issues in a few key function blocks, such as Tx and Rx chains, slope equalizer, LO generation as well as multifunction integration, will be discussed.

II. CHIPSET OVERVIEW

The functional block diagram of the Tx/Rx RFICs is shown in Fig. 1. On the transmission side, 4-bit data signal at 31MHz or 310MHz clock rate is sent to Tx IC the D/A block to generate 4-level analog I and Q signals. The analog signal goes through off-chip base-band filters for waveform shaping to limit transmission bandwidth. On-chip switch is used here for filter selection to provide flexibility in transmission speed of 100Mbps or 1Gbps



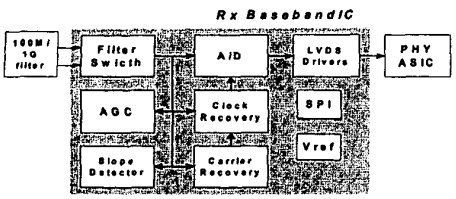


Fig.2. Conceptual block diagram of the Tx and Rx ICs

Then, the wave-shaped I/Q signal will be up-converted to RF domain via an IQ modulator. This RF signal will be amplified via a variable gain amplifier and Tx amplifier, and transmitted to the cable through a frequency multiplexer. The 90° phase difference of LO signals for I/Q modulator is provided by a frequency-divider using flip-flop circuit. A VCO circuit with switching tank circuits is used to cover the wide frequency range, and an on-chip multiplier is available that can also be switched in the LO path to allow high frequency operation. A feedback circuit was designed to control VCO's output duty cycle at 50% to ensure a precise 90° phase difference at flip-flop output. Also present on chip is a crystal oscillator circuitry (XO), synchronized to an external 19.4MHz crystal. The signal then phase-locks a 155MHz reference source on chip, which in turn is used for data generation as well as RF VCO synchronization via external PLL.

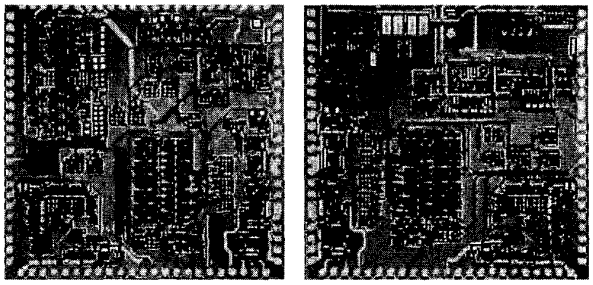
The received RF signal enters the Rx chip via a gain switching LNA. Then, a voltage control gain amplifier is used to maintain constant output level of the entire Rx chain via an AGC loop. The Rx signal then enters a slope-equalization circuit to adaptively correct the amplitude roll-off at high frequency. The RF signal will go through an I/Q demodulator to produce Rx base-band signal, which will be sent to external base-band filters via a filter selection switch circuit. A voltage control crystal oscillator (VCXO) in Rx chip is designed for clock synchronization and RF carrier recovery. The RF LO generation circuit was designed in a similar fashion as it is in Tx chip for simplicity.

As shown in Fig.2, the Rx signal will finally reach the base-band processor IC for clock recovery, carrier locking, AGC, slope detection, and conversion back to digital data. However, the details of this chip will not be discussed in this paper due to length limitation.

A 12 bit SPI control circuit was designed on both Tx/Rx chip for selection of data speed, channel frequency, gain states, power down and so on.

The SiGe HBT bipolar process was chosen for the chipset design in order to achieve flat frequency response across broad bandwidth, with low noise, high linearity and low current. The size for Tx and Rx chips are 3.9x3.9mm^2, 3.9x3.9mm^2 and 4.4x4.4mm^2, which are packaged using 7mm MLF and TQFP plastic packages. With 5Volts supply, current consumption is 310mA and 300mA for Tx and Rx chip, respectively. Photographs of the chips are depicted in Fig.3.

Since a wide variety of signals are present in each chip, including signals from fast digital data, RF carrier, crystal oscillator and clock, as well as phase lock loop components, great care was taken in circuit and layout designs to avoid interference with function blocks. Differential and symmetric circuit designs were used as much as possible to confine signal leakage. Also, supply



Tx chip(Cheetah) *Rx Chip (Zebra 1)*

Fig.3 Chipset photos

and ground lines are carefully distributed among blocks to avoid signal coupling. In terms of chip layout, location of each function block was optimized to avoid most harmful interference. In addition, isolation structures and separation spaces were carefully planned at sensitive locations.

III. Tx RF CHAIN

The building blocks of the RF transmit chain can be seen in the Fig. 4. A Gilbert cell I/Q modulator is followed by two cascaded parallel-pairs of amplifiers. Each pair consists of two differential amplifiers with different degenerations, whereby only one of the amplifiers is turned on at a time. Using this arrangement four gain states

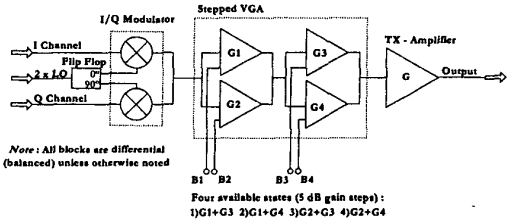
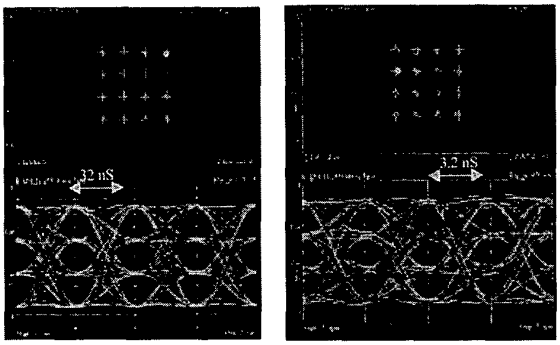


Fig.4 Function block diagram of Tx-chain

arise which were designed to offer the ability to step the output signal by 5 dB steps. In practice, at 1 GHz the steps were on the order of 4.5 dB and at 2GHz approximately 4 dB per step. The stepped-gain amplifier is followed by a power amplifier. This last on-chip amplification stage

consists of two Darlington configuration amplifiers driven in parallel by a differential amplifier buffer stage. The Darlington open collectors are pinned out with 50Ω output impedance, and an external transformer is used to combine their outputs in order to transition from a differential to a single ended signal. With a base-band input of approximately 300mVp-p, the Tx-chain will output a maximum of 7dBm (into a 50 Ohm load) at 1 GHz with 29.5 dBm OIP3. The gain roll-off from 900MHz to 2.1 GHz is less than 5dB for the entire Tx RF chain. The total DC current drain in this RF chain is approximately 155 mA at 5Volts.



100Mbps *1Gbps*

Fig.5 Constellation and eye-diagram of 100Mbps and 1Gbps Tx signals in Narad Channel 1 and Narad Channel 3. A high-speed Agilent Vector Signal Analyzer was used to measure the Tx signals.

As a representative of the Tx RFIC performance, Fig.5 depicts the constellation and eye-diagram of transmission signals for both 100Mbps and 1Gbps data speeds. The Tx signal has less than 1° quadrature phase error, and I/Q offset is lower than 50dB via offset control. Clearly, high quality signal in terms of S/N ratio, orthogonality and symmetry has been achieved using the Tx RFIC.

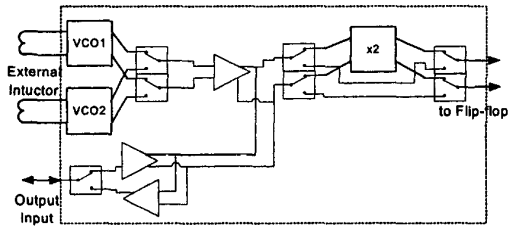


Fig.6 Concept ional function block diagram of LO signal generation.

IV. RF SIGNAL GENERATION

The broad RF bandwidth used in the high-speed data transmission creates significant frequency spacing between the 4 RF channels (940MHz, 1.05GHz, 1.35GHz, 2.1GHz). Furthermore, since a frequency divider is used in the system to generate I/Q LO signals for I/Q modulator/demodulator, the LO generation function block is required to output 2nd harmonic of the actual LO signal. Thus, a circuit configuration was designed to meet this challenge in LO generation, which is shown in Fig.6. In this circuit, a pair of differential switching VCO circuits was designed: VCO1 and VCO2 operate at the fundamental frequencies of Ch3 and Ch4, of which the signals will be frequency doubled for I/Q generation; whereas VCO2 also oscillates at the 2nd harmonics of Ch1 and Ch2, which will then be directly output without going through frequency-doubling. The LO signals are also coupled to a driver amplifier to output to external PLL circuitry. In order to provide additional flexibility, the output port for PLL can be reconfigured as an input port for external LO signals. The entire LO generation block was designed using differential circuits to prevent LO signal leakage into Tx/Rx amplifiers. Colpitts oscillator configuration and external inductors are used to achieve low phase noise, and reduce the level of interference signal generation. Fig.7 shows the excellent phase noise performance of LO signal for Ch1, which phase locked to the on-chip crystal oscillator and clock signal.

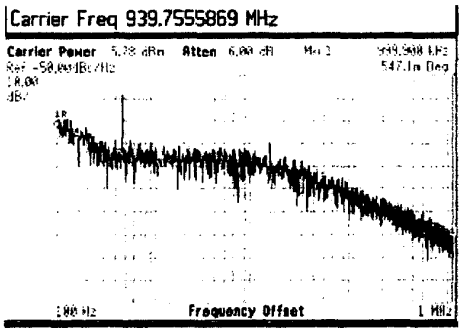


Fig.7 Phase noise performance of LO signal for Ch1, as a function of offset carrier frequencies. Mark in the plot shows that less than 1° rms phase noise is achieved.

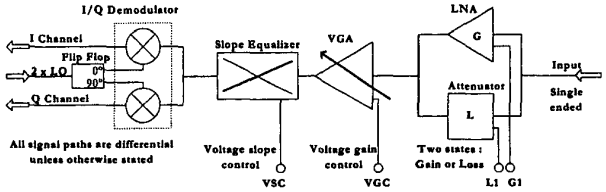


Fig.8 Receiver RF chain block diagram.

V. Rx RF CHAIN

The receiver RF functional blocks can be seen in Fig. 8. The input circuitry consists of two differential amplifier stages in parallel where only one is on at a given time. One stage provides a voltage gain of 12 dB and the other loss of 7 dB (high degeneration). This gain switch stage is critical in providing a wide receiving dynamic range to ensure high S/N ratio and low distortion when the modem is used in a variety of cable plants. While this circuit is differential, one of the input pins is AC shorted to transform the received signal from single ended to balanced signal.

The next block consists of a two-stage VGA. Current steering approach is used to control the gain of two cascaded stages of amplifiers. Approximately 40 dB of gain control is realized with a max voltage gain of 18 dB. The control voltage varies from 0 to 4.5 Volts, which is provided by the AGC circuit in the baseband processor IC.

A variable slope equalizer follows the VGA. As one may notice that, due to the wide frequency bandwidth used for 1Gbps data, the amplitude slope as a function frequency can significantly contribute to the BER in a 16QAM RF channel. Thus correcting this slope is of utmost importance. With a slope control voltage from 0 to 4.5 Volts this circuit can compensate for 12 dB of slope in the 1 to 2.5 GHz band, as shown in Fig. 9.

The equalizer circuit consists of two parallel paths. One provides flat gain frequency response while the other creates a positive slope with frequency. The positive slope is achieved via a shunt capacitor resonance tuned above 2.5 GHz. The two paths are blended at various control voltages to achieve a variable positive slope.

Finally a "Gilbert" cell I/Q demodulator is used. The receiver is designed to maintain a 600mVp-p differential signal at the base-band output with both third-order product suppression and SNR better than 30 dB within the circuit's dynamic range. The receiver dynamic range is 40 dB with a maximum allowed input RF power of 0 dBm. At maximum gain the noise figure of the Rx chain (RF to baseband) is 20dB. The DC current consumption for this RF chain is approximately 140 mA with 5Volts supply.

The modem circuit has been designed and developed using this chipset as a complete transceiver. The Narad base-band processor, PLL circuitry and filters are also in the modem. Fig. 10 shows the received base-band signal, recovered from the 100Mbps and the 1Gbps. Note that high quality Rx I/Q signals in orthogonality, symmetry, and clearance between states have been obtained. The bigger state spot in the 1Gbps case is clearly due to the limitation of the oscilloscope speed, which captures unnecessary trajectories in 1nS span. For the 100Mbps transmission between a pair of modems with the chipset, BER at 10^{-11} has been demonstrated.

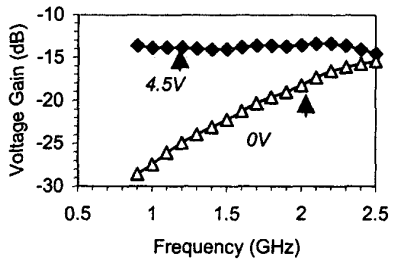


Fig.9 Variable slope equalizer response. RF and LO are swept while maintaining a small constant frequency difference between them. The base-band output level is recorded at each input RF-frequency point.

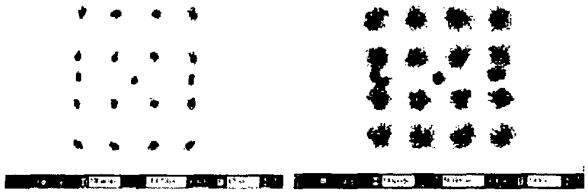


Fig.10 Constellation received of 100Mbps and 1Gbps base-band in Narad Channel 1 and Narad Channel 3(The three additional states in I channel are due to the signals for time

VI. CONCLUSIONS

We have presented the performance highlights and topology of a broadband SiGe RFIC transceiver chip-set used by Narad Networks to establish 100MBps and 1GBps digital data links in the 900 MHz to 2.5 GHz cable band. The RFIC's were designed with maximum versatility in mind to accommodate variations and changes in the system link-budget.

ACKNOWLEDGEMENT

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